



4-Channel Low Capacitance ESD Protection Arrays

CM1225

Features

- Four channels of ESD protection
- Provides ESD protection to IEC61000-4-2 Level 4
 - $\pm 8\text{kV}$ contact discharge
- Low channel input capacitance of 0.8pF (typically)
- Channel input capacitance matching (I/O to I/O) of 0.02pF (typically) is ideal for differential signals
- Minimal capacitance change for temperature and voltage
- Zener diode eliminates the need for external bypass capacitors
- Each I/O pin can withstand over 1000 ESD strikes*
- Available in a RoHS compliant (lead-free) package

Applications

- HDMI ports, DVI ports in notebooks, set top boxes, digital TVs, and LCD displays
- Display and MDDI ports
- Serial ATA ports in desktop PCs and hard disk drives
- PCI Express ports
- USB2.0 ports at 480Mbps in desktop PCs, notebooks and peripherals
- IEEE1394 FireWire ports at 400Mbps / 800Mbps
- General purpose high-speed data line ESD protection
- Protection of interface ports or IC pins which are exposed to high ESD levels

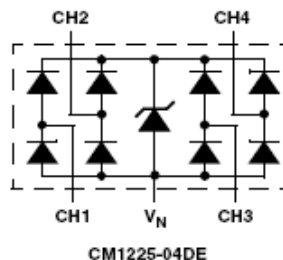
Product Description

The CM1225 diode array has been designed to provide ESD protection for electronic components or subsystems requiring minimal capacitive loading. This device is ideal for protecting systems with high data and clock rates or for circuits requiring low capacitive loading. Each ESD channel consists of a pair of diodes in series which steer the positive or negative ESD current pulse to the ground pins (V_N). A Zener diode is embedded between the positive terminal of the diode pair to the ground. This eliminates the need for an external bypass capacitor to absorb positive ESD strikes to ground. The CM1225 protects against ESD pulses up to $\pm 8\text{kV}$ per the IEC 61000-4-2 standard.

The CM1225 is particularly well-suited for protecting systems using high-speed ports such as HDMI, DVI, display, MDDI, USB 2.0, Serial ATA, IEEE1394 (FireWire and i.LINK), corresponding ports in removable storage, digital camcorders, DVD-RW drives and other applications where extremely low loading capacitance with ESD protection are required in a small package footprint.

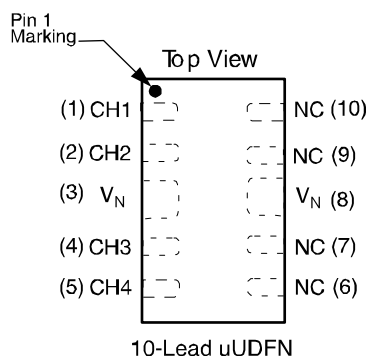
The CM1225 is available in a RoHS-compliant, uUDFN 10-pin package.

Electrical Schematic



*Standard test condition is IEC61000-4-2 level 4 test circuit with each pin subjected to $\pm 8\text{kV}$ contact discharge for 1000 pulses. Discharges are timed at 1 second intervals and all 1000 strikes are completed in one continuous test run. The part is then subjected to standard production test to verify that all of the tested parameters are within spec after the 1000 strikes.

PACKAGE / PINOUT DIAGRAMS



Note: This drawing is not to scale.

Pin Descriptions

4-CHANNEL, 10-LEAD, uUDFN-10 PACKAGE

Pin	Name	Type	Description
1	CH1	I/O	ESD Channel
2	CH2	I/O	ESD Channel
3	V _N	GND	Ground
4	CH3	I/O	ESD Channel
5	CH4	I/O	ESD Channel
6	NC		No Connect
7	NC		No Connect
8	V _N	GND	Ground
9	NC		No Connect
10	NC		No Connect



4-Channel Low Capacitance ESD Protection Arrays

CM1225

Ordering Information

PART NUMBERING INFORMATION				
# of Channels	Leads	Package	Lead-free Finish	
			Ordering Part Number ¹	Part Marking
4	10	uUDFN-10	CM1225-04DE	1225

Note 1: Parts are shipped in Tape and Reel form unless otherwise specified.

Specifications

ABSOLUTE MAXIMUM RATINGS		
PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C
Storage Temperature Range	-65 to +150	°C
DC Voltage at any channel input	- 0.5 to 5.5	V

STANDARD OPERATING CONDITIONS		
PARAMETER	RATING	UNITS
Operating Temperature Range	-40 to +85	°C

ELECTRICAL OPERATING CHARACTERISTICS (SEE NOTE 1)

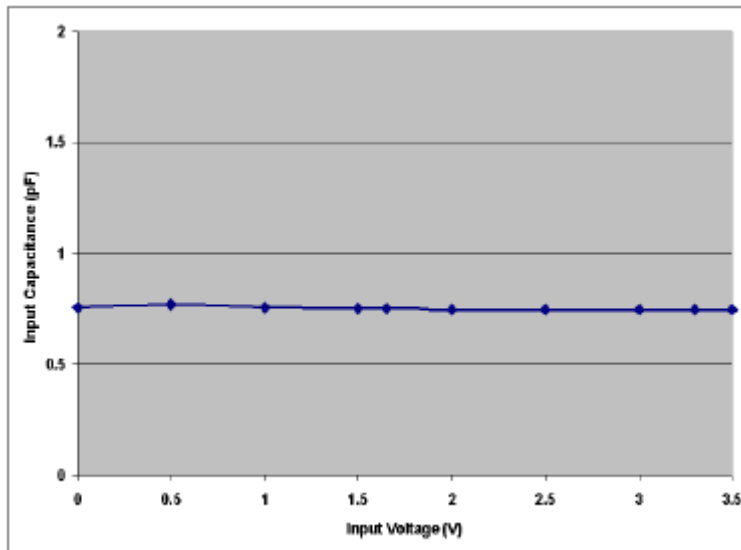
SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
V_F	Diode Forward Voltage Top Diode Bottom Diode	$I_F = 10\text{mA}$; $T_A = 25^\circ\text{C}$; Note 2	0.65	0.85	1.20	V
			-1.20	-0.85	-0.65	V
I_{LEAK}	Channel Leakage Current	$T_A = 25^\circ\text{C}$; $V_{IN} = 3.3\text{V}$, $V_N = 0\text{V}$		± 0.1	± 1.0	μA
C_{IN}	Channel Input Capacitance	At 1 MHz, $V_N = 0\text{V}$, $V_{IN} = 1.65\text{V}$		0.80	1.0	pF
ΔC_{IN}	Channel Input Capacitance Matching	At 1 MHz, $V_N = 0\text{V}$, $V_{IN} = 1.65\text{V}$		0.02		pF
V_{ESD}	ESD Protection - Peak Discharge Voltage at any channel input, in system: Contact discharge per IEC 61000-4-2 standard	$T_A = 25^\circ\text{C}$; Notes 2 and 3		± 8		kV
V_{CL}	Channel Clamp Voltage Positive Transients Negative Transients	$T_A = 25^\circ\text{C}$, $I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{S}$; Note 3		+10.0		V
				-4.5		V
R_{DYN}	Dynamic Resistance Positive Transients Negative Transients	$I_{PP} = 1\text{A}$, $t_p = 8/20\mu\text{S}$ Any I/O pin to Ground; Note 3		1.3		Ω
				1.3		Ω

Note 1: All parameters specified at $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ unless otherwise noted.
 Note 2: Standard IEC 61000-4-2 with $C_{Discharge} = 150\text{pF}$, $R_{Discharge} = 330\Omega$, V_N grounded.
 Note 3: These measurements performed with no external capacitor.



Performance Information

Input Channel Capacitance Performance Curves



Performance Information (cont'd)

Typical Filter Performance (nominal conditions unless specified otherwise, 50 Ohm Environment)

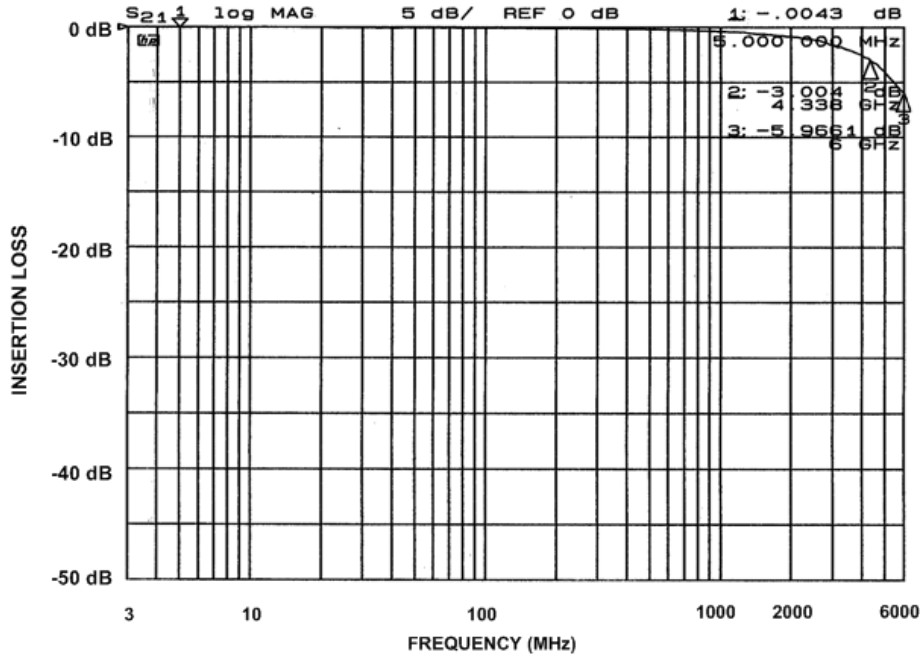


Figure 1. Insertion Loss (S21) VS. Frequency (0V DC Bias)

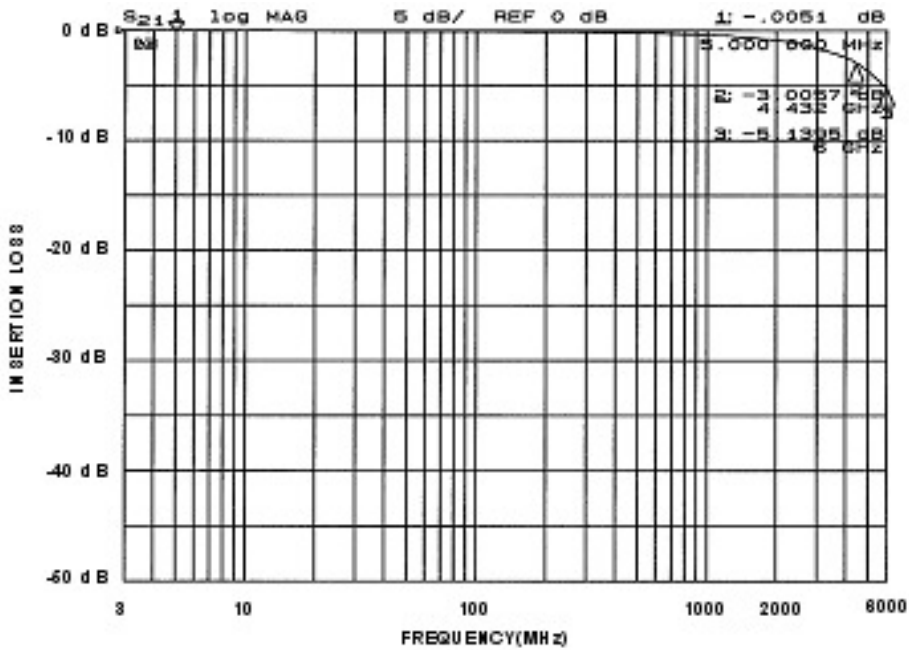


Figure 2. Insertion Loss (S21) VS. Frequency (2.5V DC Bias)



Application Information

Design Considerations

As a general rule, the CM1225 ESD protection array should be located as close as possible to the point of entry of expected electrostatic discharges. Use minimum PCB trace lengths to ground planes and between the signal input and the ESD devices.

Additional Information

See also California Micro Devices Application Note AP209, "Design Considerations for ESD Protection," in the Applications section at www.calmicro.com.

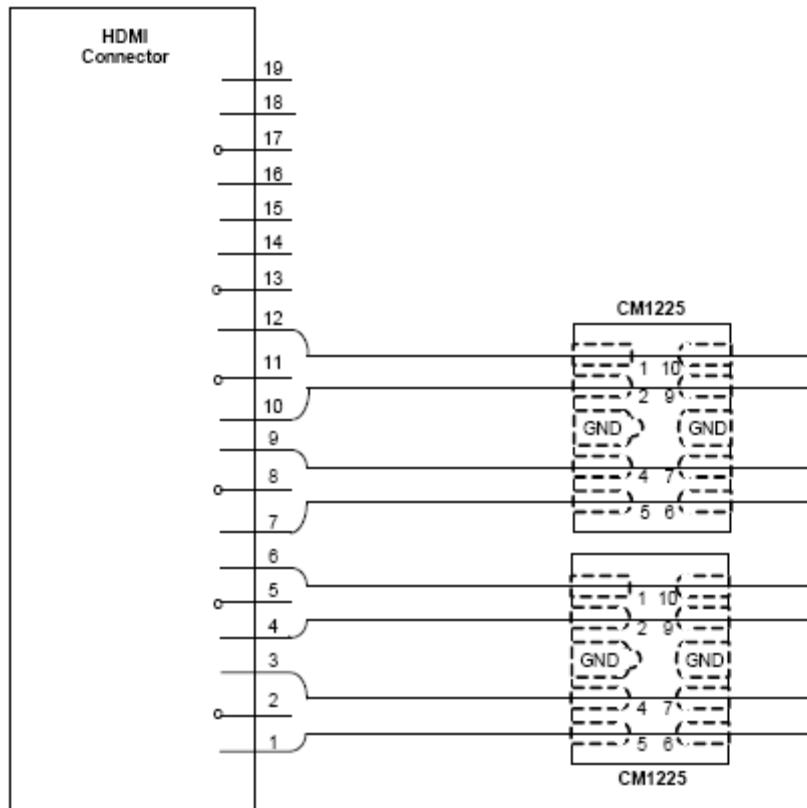


Figure 3. Typical HDMI ESD Protection with CM1225 Connection

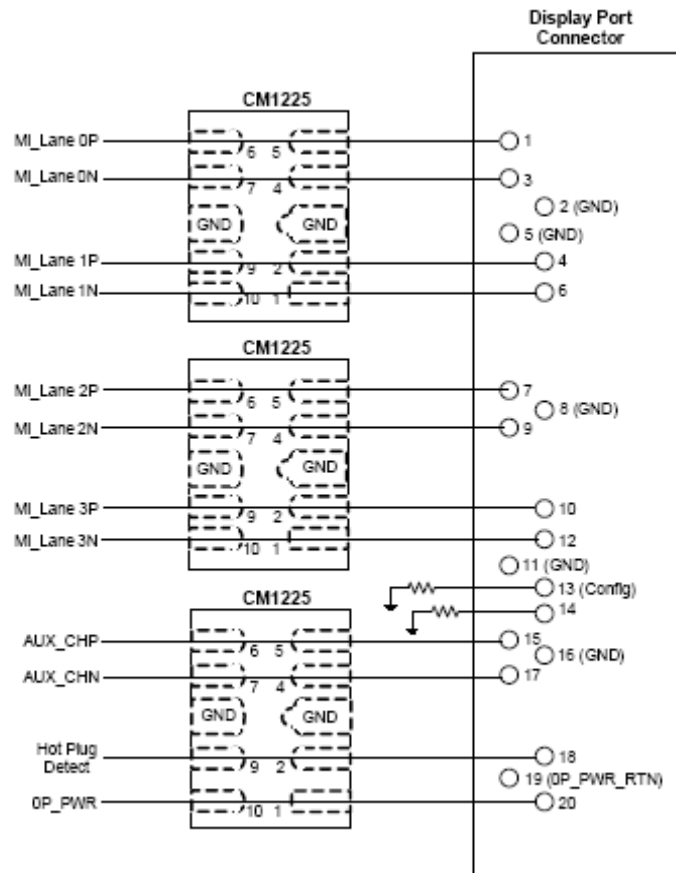


Figure 4. Display Port ESD Protection with CM1225 Connection



4-Channel Low Capacitance ESD Protection Arrays

CM1225

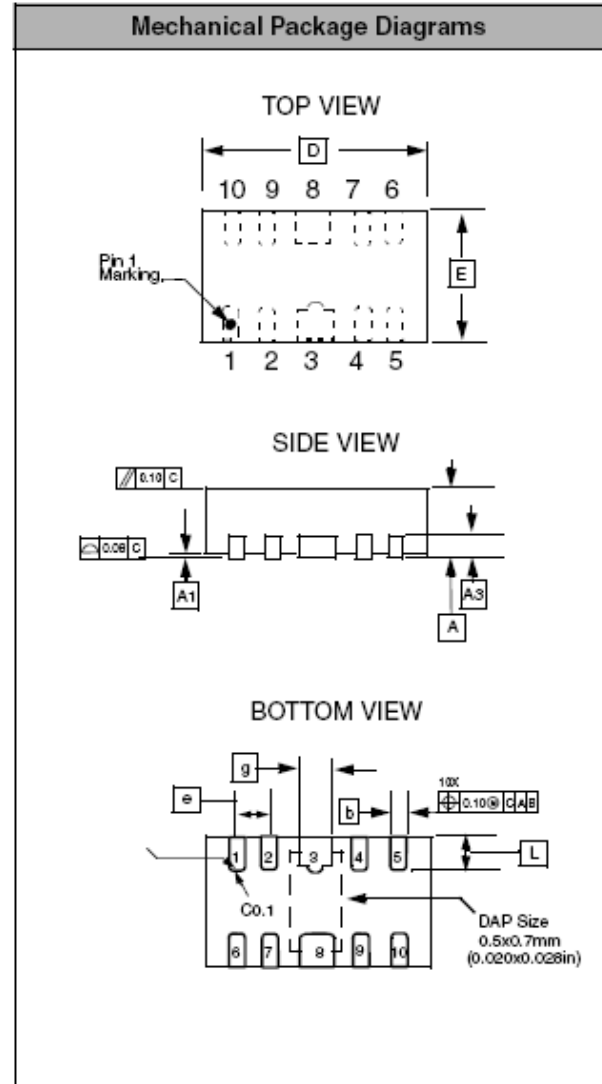
Mechanical Details

uUDFN-10 Mechanical Specifications, 0.5mm

The 10-lead, 0.5mm pitch uUDFN package dimensions are presented below.

PACKAGE DIMENSIONS						
Package	uUDFN					
JEDEC No.	MO-229C*					
Leads	10					
Dim.	Millimeters			Inches		
	Min	Nom	Max	Min	Nom	Max
A	0.45	0.50	0.55	0.180	0.020	0.022
A1	0.00	0.02	0.05	0.000	0.001	0.002
A3	0.102	0.127	0.152	0.004	0.005	0.006
b	0.15	0.20	0.25	0.006	0.008	0.010
D	2.40	2.50	2.60	0.095	0.098	0.102
E	0.90	1.00	1.10	0.035	0.039	0.043
e	0.50 BSC			0.020 BSC		
g	0.35	0.40	0.45	0.014	0.016	0.018
L	0.30	0.35	0.40	0.012	0.014	0.016
# per tape and reel	3000 pieces					
Controlling dimension: millimeters						

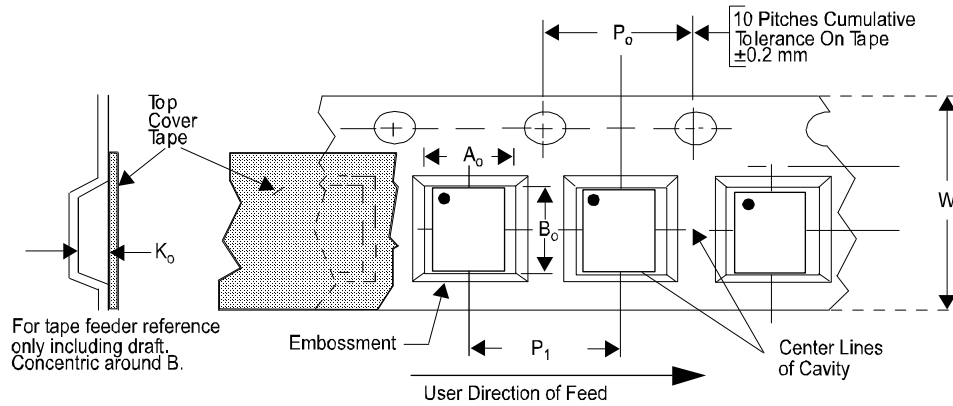
* This package is compliant with JEDEC standard MO-229C with the exception of the D and E dimensions as called out in the table above.



Dimensions for 10-Lead, 0.5mm Pitch uUDFN Package

Tape and Reel Specifications


PART NUMBER	PACKAGE SIZE (mm)	POCKET SIZE (mm) $B_o \times A_o \times K_o$	TAPE WIDTH W	REEL DIAMETER	QTY PER REEL	P_o	P_1
CM1225	2.50 X 1.00 X 0.50	2.80 X 1.45 X 0.70	8mm	178mm (7")	3000	4mm	4mm





4-Channel Low Capacitance ESD Protection Arrays

CM1225

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor

P.O. Box 5163, Denver, Colorado 80217 USA

Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada

Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada

Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855

Toll Free USA/Canada

Europe, Middle East and Africa Technical Support:

Phone: 421 33 790 2910

Japan Customer Focus Center

Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative